LIST OF THE CLAIMS

1-40. (Canceled)

41. (Currently Amended): A method of fabricating a thin film transistor, comprising:

forming a gate insulating layer on an active layer;

forming a gate on the gate insulating layer;

forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask; and

forming an impurity region by implanting impurity ions to said excited region in a heavy dosage while the excited region remains in an excited state, whereby the implanted impurity ions become self-activated.~~whereby a post-heat treatment for activation of the impurity ions is eliminated from the method of fabricating the thin film transistor~~ .

42. (Previously Presented): The method of claim 41, wherein the gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate.

43. (Previously Presented): The method of claim 41, wherein the active layer is formed by depositing undoped polycrystalline silicon.

44. (Previously Presented): The method of claim 43, wherein the undoped polycrystalline silicon has a thickness of between about 400 and 800 Å.

45. (Previously Presented): The method of claim 43, wherein the active layer is formed using chemical vapor deposition process.

46. (Previously Presented): The method of claim 41, wherein the active layer is formed by depositing amorphous silicon and crystallizing the amorphous silicon by laser annealing.

47. (Previously Presented): The method of claim 41, wherein the exposed portion of the active layer is formed by the steps of depositing an another layer of silicon dioxide on the gate insulating layer to cover the active layer; depositing a conductive material on the another layer of silicon dioxide; and patterning the conductive material and the another layer of silicon dioxide to form an insulating layer and to form the gate over a selected portion of the active layer.

48. (Previously Presented): The method of claim 47, wherein the gate insulating layer and the gate comprise a thickness of about 500-1500 Å and, about 1500-2500 Å, respectively.

49. (Previously Presented): The method of claim 41, wherein said hydrogen ions are implanted with implantation energy between about 50 and 150 KeV.

50. (Previously Presented): The method of claim 41, wherein said hydrogen ions are implanted with a dose of between about 5×10^{14} - 5×10^{16} ions/cm^2.

51. (Previously Presented): The method of claim 49, wherein said hydrogen ions are implanted to heat up the excited region to a temperature between about 200-300 degrees Celsius.

52. (Previously Presented): The method of claim 50, wherein said hydrogen ions are implanted to heat up the excited region to a temperature between about 200-300 degrees Celsius.

53. (Previously Presented): The method of claim 41, wherein said hydrogen ions are implanted in the active layer and simultaneously form the impurity region.

54. (Previously Presented): The method of claim 41, wherein the hydrogen ion implantation time is proportionately related to the size of the active layer.

55. (Previously Presented): A thin film transistor prepared by a process comprising:

forming a gate insulating layer on an active layer;

forming a gate on the gate insulating layer;

forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask; and

forming an impurity region by implanting impurity ions to said excited region while the excited region remains in an excited state, wherein the activation of said impurity ions implanted occurs as the step of said implanting impurity ions is performed.

56. (Previously Presented): The thin film transistor of claim 55, wherein the gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate, and the active layer is formed by depositing undoped polycrystalline silicon.